WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

a first circuit formed on the semiconductor substrate, the first circuit including first and second field-effect transistors,

the first field-effect transistor comprising:

a first source region and a first drain region formed apart from each other on a surface of the semiconductor substrate;

a first gate insulation film formed between the first source region and the first drain region; and

a first gate electrode formed on the first gate insulation film,

the second field-effect transistor comprising:

a second source region and a second drain region formed apart from each other and apart from the first field-effect transistor on the surface of the semiconductor substrate;

a second gate insulation film formed between the second source region and the second drain region; and

a second gate electrode formed on the second gate insulation film,

the first drain region of the first field-effect transistor accompanying a first load capacitance,

the second drain region of the second field-effect

transistor accompanying a second load capacitance which is smaller than the first load capacitance, and the first gate insulation film of the first field-effect transistor having an average relative dielectric constant higher than that of the second gate insulation film of the second field-effect transistor, and

a second circuit coupled to the first circuit as an input/output portion of the first circuit and powered by a voltage higher than that for the first circuit.

2. The semiconductor device according to claim 1, wherein the first field-effect transistor of the first circuit drives the second circuit.

3. The semiconductor device according to claim 1, wherein the first gate insulation film of the first field-effect transistor is formed of a mixture of amorphous material and crystalline material, and the second gate insulation film of the second field-effect transistor is substantially formed of the amorphous material.

4. The semiconductor device according to claim 3, wherein the crystalline material is a metal oxide.

5. The semiconductor device according to claim 1, wherein the first gate insulation film and the second gate insulation film are formed of a mixture of amorphous material and crystalline material, and an amount of the crystalline material in the first gate

insulation film is larger than that of the crystalline material in the second gate insulation film.

6. The semiconductor device according to claim 5, wherein the crystalline material is a metal oxide.

7. The semiconductor device according to claim 1, wherein the first gate insulation film and the second gate insulation film include silicon, oxygen, and a metal element.

8. The semiconductor device according to claim 7, wherein a ratio of the number of atoms of the metal element included in the first gate insulation film to a sum of the numbers of atoms of the metal element and the silicon is 0.3 or more.

9. The semiconductor device according to claim 7, wherein a ratio of the number of atoms of the metal element included in the second gate insulation film to a sum of the numbers of atoms of the metal element and the silicon is 0.1 or less.

10. The semiconductor device according to claim 7, wherein a ratio of the number of atoms of the metal element included in the second gate insulation film to a sum of the numbers of atoms of the metal and the silicon is 0.3 or more, and a ratio of an average radius of an oxide of the metal to a thickness of the second gate insulation film is 0.1 or less.

11. A manufacturing method of a first and a second field-effect transistors comprising:

disposing a plurality of isolation regions in a semiconductor substrate to define first and second well forming regions;

implanting an impurity of a first conductivity type into the first and the second well forming regions to form first and second well regions of the first conductivity type;

forming a gate insulation film in a surface of the first and the second well regions;

selectively forming a nitrogen diffusion preventive film on the gate insulation film of the first well region;

exposing the first and the second well regions to a nitrogen-containing atmosphere;

after removing the nitrogen diffusion preventive film, forming a polycrystalline silicon film on the gate insulation film on the first and the second well regions;

selectively and anisotropically etching the polycrystalline silicon film to form first and second gate electrodes on the gate insulation film on the first and the second well regions; and

forming first and second pair of source/drain regions by implanting and thermally diffusing an impurity of a second conductivity type in the first and the second well regions, using the first and the second gate electrodes as masks, respectively.

12. The manufacturing method according to claim 11, wherein the gate insulation film includes silicon, oxide, and a metal element.

13. The manufacturing method according to claim 12, wherein the forming of a first and a second pair of source/drain regions includes precipitating an oxide of the metal element in the gate insulation film on the first well region.

14. A manufacturing method of a first and a second field-effect transistors comprising:

forming first and second well forming regions separated by a plurality of isolation regions in a semiconductor substrate;

forming first and second well regions of a first conductivity type by implanting an impurity of a first conductivity type into the first and the second well forming regions;

forming a first gate insulation film on the first and the second well regions;

introducing nitrogen into the first gate insulation film by exposing the first gate insulation film to a nitrogen-containing atmosphere;

selectively removing the first gate insulation film on the first well region;

newly forming a second gate insulation film on the first well region;

forming a polycrystalline silicon film on the

first and the second well regions via the first and the second gate insulation films;

forming first and second gate electrodes above the first and the second well regions by selectively and anisotropically etching the polycrystalline silicon film; and

forming a first and a second pair of source/drain regions by implanting and thermally diffusing an impurity of a second conductivity type into the first and the second well regions, using the first and the second gate electrodes as masks, respectively.

15. The manufacturing method according to claim 14, wherein the first and the second gate insulation film include silicon, oxygen, and a metal element.

16. The manufacturing method according to claim 15, wherein the forming of a first and a second pair of source/drain regions includes precipitating an oxide of the metal element in the gate insulation film on the first well region.

17. A manufacturing method of a first and a second field-effect transistors comprising:

forming a first and a second well forming region separated by a plurality of isolation regions in a semiconductor substrate;

forming a first and a second well regions of a first conductivity type by implanting an impurity of

a first conductivity type into the first and the second well forming regions;

forming a first gate insulation film on the first and the second well regions;

selectively forming a nitrogen diffusion preventive film above the surface of the first well region;

removing the first gate insulation film on the second well region by using the nitrogen diffusion preventive film as a mask;

newly forming a second gate insulation film on the first and the second well regions;

introducing nitrogen into the second gate insulation film;

removing the second gate insulation film and the nitrogen diffusion preventive film on the first well region;

after removing the nitrogen diffusion preventive film, forming a polycrystalline silicon film on the first and the second well regions via the first and the second gate insulation films;

forming a first and a second gate electrodes above the first and the second well regions by selectively and anisotropically etching the polycrystalline silicon film; and

forming a first and a second pair of source/drain regions by implanting and thermally diffusing an

impurity of a second conductivity type into the first and the second well regions, using the first and the second gate electrodes as masks, respectively.

18. The manufacturing method according to claim 17, wherein the first and the second gate insulation films includes silicon, oxygen, and a metal element.

19. The manufacturing method according to claim 18, wherein the forming step of a first and a second pair of source/drain regions includes precipitating an oxide of the metal element in the gate insulation film on the first well region.

20. A manufacturing method of a first and a second field-effect transistors comprising:

forming a first and a second well forming regions separated by a plurality of isolation regions in a semiconductor substrate;

forming a first and a second well regions of a first conductivity type by implanting an impurity of a first conductivity type into the first and the second well forming regions;

forming a first gate insulation film on the first and the second well regions;

removing the first gate insulation film on the second well region;

newly forming a second gate insulation film on the second well region;

forming a polycrystalline silicon film on the first and the second well regions via the first and the second gate insulation films;

forming a first and a second gate electrodes above the first and the second well regions by selectively and anisotropically etching the polycrystalline silicon film; and

forming a first and a second pair of source/drain regions by implanting and thermally diffusing an impurity of a second conductivity type into the first and the second well regions, using the first and the second gate electrodes as masks, respectively.